IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, all list of all claims are included below.

1. (Currently amended) A method for diagnosing programmable hardware comprising:

recognizing an occurrence of a user-specified event;

generating a signal to cease bus access, in a configurable system on a chip, upon the occurrence of ~~a~~ the user-specified event, the configurable system on a chip integrating at least a central processing unit, an internal system bus, and a configurable logic, the signal generated by a breakpoint unit connected to the internal system bus, such that the breakpoint unit can be programmed through a debug port;

allowing completion of all pending bus transactions;

stopping the system clock such that the state of the hardware is held static; and

accessing the static state of the hardware through ~~a~~ the debug port.

2. (Previously presented) The method of claim 1, wherein the internal system bus is a pipeline bus.

3. (Original) The method of claim 1, wherein the debug port is a bus master.

4. (Original) The method of claim 1, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

5. (Original) The method of claim 4, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

6. (Previously presented) The method of claim 1, wherein the user-specified event is programmed by a user.

7. (Currently amended) A machine-readable medium that provides executable instructions, which when executed by a processor, cause said processor to perform a method for diagnosing programmable hardware comprising:

recognizing an occurrence of a user-specified event;

generating a signal to cease ~~ceasing~~ bus access, in a configurable system on a chip, upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit, an internal system bus, and a configurable logic, the signal generated by a breakpoint unit connected to the internal system bus, such that the breakpoint unit can be programmed through a debug port;

allowing completion of all pending bus transactions;

stopping the system clock such that the state of the hardware is held static; and

accessing the static state of the hardware through ~~a~~ the debug port.

8. (Previously presented) The machine-readable medium of claim 7, wherein the internal system bus is a pipeline bus.

9. (Original) The machine-readable medium of claim 7, wherein the debug port is a bus master.

10. (Original) The machine-readable medium of claim 7, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

11. (Original) The machine-readable medium of claim 10, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

12. (Previously presented) The machine-readable medium of claim 7, wherein the user-specified event is programmed by a user.

13. (Currently amended) An apparatus for diagnosing programmable hardware comprising:

means to recognize an occurrence of a user-specified event;

a breakpoint unit ~~means~~ to generate a signal to cease bus access, in a configurable system on a chip, upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit, an internal system bus, and a configurable logic, the breakpoint unit connected to the internal system bus, such that the breakpoint unit can be programmed through a debug port;

means to allow completion of all pending bus transactions;

means to stop the system clock such that the state of the hardware is held static; and

means to access the static state of the hardware through ~~a~~ the debug port.

14. (Previously presented) The apparatus of claim 13, wherein the internal system bus is a pipeline bus.

15. (Original) The apparatus of claim 13, wherein the debug port is a bus master.

16. (Original) The apparatus of claim 13, wherein allowing completion of all pending bus transactions includes monitoring the bus for pending bus transactions.

17. (Original) The apparatus of claim 16, wherein allowing completion of all pending bus transactions further includes generating a qualified clock freeze cycle upon completion of all pending bus transactions.

18. (Previously presented) The apparatus of claim 13, wherein the user-specified event is programmed by a user.

19. (Previously presented) The method of claim 6 wherein the user-specified event comprises a sequence of events.

20. (Previously presented) The machine-readable medium of claim 16 wherein the user-specified event comprises a sequence of events.

21. (Previously presented) The apparatus of claim 18 wherein the user-specified event comprises a sequence of events.

22. (New) The method of claim 1 wherein the breakpoint unit is connected to a plurality of buses such that the breakpoint unit generates a signal in response to a user-specified event on any of the plurality of buses.

23. (New) The method of claim 22 wherein the breakpoint unit is programmed to generate multiple signals upon the occurrence of a user-specified event.